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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re application of:	
Ki-Young LEE, et al.	Examiner: Paul E. Brock II
Serial No. 09/389,491	Group Art Unit: 2815
Filed: September 3, 1999	
For: Semiconductor Integrated Circuit Capacitor and Method for Fabricating Same	Date: September 11, 2003

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APPENDIX A

THE CLAIMS ON APPEAL

12. (Five Times Amended) A method of manufacturing a semiconductor integrated circuit capacitor, comprising:

providing an insulating substrate;

simultaneously forming a first wire line and a lower electrode on predetermined surfaces of the insulating substrate;

forming an interlevel insulating layer on the substrate, on the first wire line, and on the lower electrode;

selectively etching the interlevel insulating layer to expose a predetermined surface of the lower electrode and a predetermined surface of the first wire line thereby simultaneously forming in the interlevel insulating layer: (i) a first via hole having sidewalls and disposed above the lower electrode; and (ii) a second via hole disposed above the first wire line;

forming a tungsten containing conductive layer on the interlevel insulating layer and in the first and second via holes, including on the exposed predetermined surfaces of the lower electrode and first wire line;

performing a tungsten etch back process to selectively etch back the tungsten containing conductive layer on the interlevel insulating layer and in the first and second via holes to simultaneously form: (i) a tungsten containing conductive sidewall spacer on the sidewalls of the first via hole and a portion of the exposed predetermined surface of the lower electrode from the tungsten containing conductive layer formed in the first via hole for preventing dielectric disconnection; (ii) a tungsten containing conductive plug in the second via hole on the predetermined surface of the first wire line from the tungsten containing conductive layer formed in the second via hole, the tungsten containing conductive sidewall spacer and the tungsten containing conductive plug being formed of the same tungsten containing conductive layer; and (iii) an exposed surface containing the spacer, conductive plug, a portion of the predetermined surface of the lower electrode not covered by the tungsten containing conductive sidewall spacer, and predetermined surfaces of the interlevel insulating layer;

forming a dielectric layer on the exposed surface, the tungsten containing conductive sidewall spacer and the tungsten containing conductive layer formed in the first via hole;

removing the dielectric layer on the exposed surface except for a predetermined portion of the dielectric layer disposed on the tungsten containing conductive sidewall spacer, and predetermined surface of the lower electrode not covered by the tungsten containing conductive sidewall spacer; and

simultaneously forming: (i) a second wire line connected to the tungsten containing

conductive plug; and (ii) an upper electrode connected to the dielectric layer.

14. The method as claimed in claim 12, wherein the dielectric layer has a structure selected from: (i) a single-level structure containing an oxide layer or nitride layer; or (ii) a multi-level structure containing layers selected from the group consisting of oxide layers, nitride layers, and mixtures thereof.

15. The method as claimed in claim 14, wherein the oxide layer is made using a deposition technique employing Plasma Enhanced Oxide (PEOX), P-SiH_4, or High Density Plasma (HDP).

16. The method as claimed in claim 14, wherein the nitride layer is made using a deposition technique employing Plasma Enhanced Nitride (PESiN).

17. The method as claimed in claim 14, wherein the multi-level structure is selected from the group consisting of an oxide/nitride layer, a nitride/oxide layer, an oxide/nitride/oxide layer and a nitride/oxide/nitride layer.

18. The method as claimed in claim 12, wherein the lower and upper electrodes are made of a material selected from an aluminum alloy, a copper alloy, and mixtures thereof.

19. The method as claimed in claim 18, further comprising an anti-reflection layer disposed on the lower and/or upper electrodes' surface.

20. (Twice Amended) The method as claimed in claim 19, wherein the anti-reflection layer has a structure selected from the group consisting of: (i) a single-level structure comprised of one or more materials selected from the group consisting of Ti, Ta, Mo, TiN, TiW, TaN, and MoN and/or (ii) a multi-level structure comprised of one or more materials selected from the group consisting of W-N, W-Si-N, Ta-Si-N, W-B-N, and Ti-Si-N.

21. The method as claimed in claim 18, further comprising a metal barrier layer disposed on the lower and/or upper electrode's surface.

22. (Twice Amended) The method as claimed in claim 21, wherein the metal barrier layer has a structure selected from the group consisting of: (i) a single-level structure comprised of one or more materials selected from the group consisting of Ti,

Ta, Mo, TiN, TiW, TaN, and MoN and/or (ii) a multi-level structure comprised of one or more materials selected from the group consisting of W-N, W-Si-N, Ta-Si-N, W-B-N, and Ti-Si-N.

23. The method as claimed in claim 12, further comprising, after forming the first and second via holes, RF sputter etching the interlevel insulating layer and the first and second via holes.

24. The method as claimed in claim 12, wherein the interlevel insulating layer is selectively etched by a process selected from the group consisting of dry-etching, wet-etching and dry/wet-combined etching.

26. The method as claimed in claim 12, wherein the spacer formed on the sidewalls of the via hole has a sloping surface.